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TO THE ASSISTANT COMMISSIONER FOR PATENTS

Transmitted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

SCOTT A. ROSENBERG and ANTHONY C. MILLER

For: LIQUID CRYSTAL OVER SEMICONDUCTOR DISPLAY WITH ON-CHIP STORAGE

jc511 U.S. PTO 09/365363 07/30/99

Enclosed are:

- ☒ Certificate of Mailing with Express Mail Mailing Label No. EL360180325US
- ☒ 3 sheets of drawings.
- ☐ A certified copy of a application.
- ☒ Declaration ☒ Signed. ☐ Unsigned.
- ☒ Power of Attorney
- ☐ Information Disclosure Statement
- ☐ Preliminary Amendment
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For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	25	- 20 =	5	x	$18.00	$90.00
Indep. Claims	5	- 3 =	2	x	$78.00	$156.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$760.00
					TOTAL FILING FEE	$1,006.00

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Dated: JULY 30, 1999

Signature

TIMOTHY N. TROP
REG. NO. 28,994
TROP, PRUNER, HU & MILES, P.C.
8554 KATY FREEWAY, STE. 100
HOUSTON, TX. 77024
713/468-8880
713/468-8883 [FAX]

cc:

INTL-0219-US
(P7127)

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: LIQUID CRYSTAL OVER SEMICONDUCTOR DISPLAY WITH ON-CHIP STORAGE

INVENTORS: SCOTT A. ROSENBERG and
ANTHONY C. MILLER

Express Mail No.: EL360180325US

Date: JULY 30, 1999

LIQUID CRYSTAL OVER SEMICONDUCTOR DISPLAY WITH ON-CHIP STORAGE

Background

This invention relates generally to displays for electronic devices such as computers.

Liquid crystal displays (LCD) are used as the displays for a large number of electronic devices including laptop computers, telephones, desktop computers, and televisions. However, the predominant display technology continues to use cathode ray tubes (CRT). Most displays today are designed to interface with the older analog technology standards.

Typical CRTs use a raster update interface. This means that pixels must be repeatedly traced in a linear fashion from left to right across the display and from top to bottom. This scanning occurs at a relatively high rate because the image elements of the CRT glow for only a short period of time. Thus, these image elements or phosphors must be frequently refreshed in order to give the appearance of constant light.

Because of the prevalence and widespread acceptance of CRTs as displays for electronic devices, most displays, including liquid crystal displays, tend to match the CRT interface paradigm. Thus, most displays are not designed to have their images persist for a relatively longer time

because the raster interface paradigm guarantees that the image is quickly refreshed.

The display refresh controller which provides the refresh signals for the display may use an interface bus that is also used by a graphics processor and general purpose microprocessor in the host system. In addition, the controller may make use of the system memory that other system level devices utilize. Thus, the continuing demands for display refresh tend to tax the available system resources. This means that some portion of the available system bandwidth must be dedicated to supporting the display refresh operation. This may adversely affect bandwidth and potentially decrease system performance.

The need to periodically refresh the information in the display takes up some of the bandwidth that could be used to increase the resolution of the display. In addition, some of the available bandwidth could be used to provide higher rate images if that bandwidth were not consumed in supplying redundant information to the display.

Summary

A display includes a semiconductor substrate. A liquid crystal over semiconductor pixel array is formed in the substrate. A memory coupled to the array is also formed in the substrate.

Brief Description of the Drawings

Fig. 1 is a schematic cross-sectional view of one embodiment of the display in accordance with the present invention;

Fig. 2 is a more detailed enlarged, cross-sectional view of a display of the type shown in Fig. 1;

Fig. 3 is a block diagram of a display in accordance with one embodiment of the present invention;

Fig. 4 is a system level block diagram of another embodiment of the present invention;

Fig. 5 is a schematic diagram of one cell of the display in accordance with another embodiment of the present invention; and

Fig. 6 is a schematic diagram of a display implementing one embodiment of the present invention.

Detailed Description

Referring to Fig. 1, an electro-optical device 10, such as a spatial light modulator (SLM), may include a plurality of reflective mirrors 12 defined on a semiconductor substrate 14 in accordance with one embodiment of the present invention. Advantageously, the device 10 is implemented using liquid crystal over semiconductor (LCOS) technology. LCOS technology may form large screen projection displays or smaller displays (using direct view rather than projection technology). With LCOS technology, the liquid crystal display is formed in

association with the same substrate that forms complementary metal oxide semiconductor (CMOS) circuit elements. The display may be a reflective liquid crystal display.

The device 10 may include a silicon substrate 14 with a metal layer defining the mirrors 12. The mirrors 12 may be the mirrors of an electro-optic display such as a liquid crystal display. For example, the mirrors 12 may be part of spatial light modulator (SLM) for one of the color planes of a tricolor display. Potentials applied to the mirrors 12 alter the liquid crystal to modulate the incoming light to create images which then can be directly viewed or projected onto a projection screen.

Referring to Fig. 2, each cell or pixel of the display may include a reflective mirror 24 forming one of the mirrors of one of the pixels 12 shown in Fig. 1. In one embodiment of the invention, each cell may be rectangular or square and a slight spacing may occur between each adjacent mirror 24. Thus, a rectangular array of mirrors 24 may form an array of pixel elements in conjunction with liquid crystal material 20 positioned over the mirrors 24.

The LCOS structure includes a silicon substrate 14 having doped regions 32 formed therein. The doped regions 32 may define transistors for logic elements and/or memory cells which operate in conjunction with the display pixels as will be described hereinafter. Four or more metal

layers may be provided, including a metal one layer 30 which is spaced by an inter-layer dielectric (ILD) 31 from a metal two layer 28 and a metal three layer 26. A metal four layer may form the pixel mirrors 24. Thus, for example, the metal two layer 28 may provide light blocking and the metal one layer may provide the desired interconnections for forming the semiconductor logic and memory devices. The pixel mirrors 24 may be coupled, by way of vias 32, with the other metal layers.

A dielectric layer 22 may be formed over the mirror 24. A liquid crystal or electro-optic material 20 is sandwiched between a pair of buffered polyimide layers 19a and 19b. One electrode of the liquid crystal device is formed by the metal layer 24. The other electrode is formed by an indium tin oxide (ITO) layer 18.

A top plate 16 may be formed of transparent material. The ITO layer 18 may be coated on the top plate 26. The polyimide layers 19a and 19b provide electrical isolation between the capacitor plates which sandwich the electro-optic material 20. However, other insulating materials may be coated on the ITO layer 18 in place of or in addition to the polyimide layers.

Using the LCOS structure, for example as depicted in Fig. 2, a memory element or array may be incorporated into the same silicon substrate which includes the pixel array. In one embodiment of the present invention, a separate

memory array 36 may be included on the same substrate 14 that includes the pixel array 42, as shown in Fig. 3. The memory array may be, for example, dynamic random access memory (DRAM).

The memory array 36 receives and transmits data, as indicated by the arrows on the left side of the array 36 from a display controller in a host processor-based system (not shown in Fig. 3). The array 36 also communicates with the pixel array 42 via a refresh circuit 38 utilized for both DRAM memory refresh and pixel array refresh. A digital to analog converter 40 converts the data from the memory 36 to an analog format for addressing particular pixels in the pixel array 42. Moreover, the refresh circuit 38 may feed back to the memory array 36 so that the refresh circuit 38 not only refreshes the pixels in the pixel array 42 but also refreshes the memory array 36.

Thus, in the process of rewriting the DRAM cells for their own refresh, the same refresh circuitry also updates the pixel cells. Since DRAM and pixel refresh cycles are combined into one cycle, the overall read bandwidth, sourced from the DRAM array, may be reduced. Compared to systems where two separate streams of data are simultaneously read out of the DRAM array, less bandwidth may be used. By using only one stream for both refresh operations, combining the memory and refresh cycles into

one cycle, the overall bandwidth required from the DRAM memory is reduced.

In refresh embodiments, flexibility may be achieved in the number of DRAM bits allocated per pixel cell. In some applications, for instance, the creation of multiple low accuracy buffers may be more advantageous than the creation of a single high accuracy buffer. Because the internal scan process produces additional margin, memory bits may be transferred to the pixel array in many ways using embodiments of the present invention.

Referring next of Fig. 4, a processor-based host system 51 for the electro-optical device 10 includes a system memory 43 which is coupled through an interface bus 44 with a general purpose microprocessor 46 in accordance with one embodiment of the invention. The interface bus 44 also may provide processor and memory access to a media or graphics processor 48 and a display refresh controller 50. The display refresh controller is coupled by a bus 49 to the electro-optic device 10 which may be an LCOS display with integrated storage.

In systems that do not modulate the liquid crystal display in an analog fashion, no digital to analog conversion may be used. Values may be read directly from the storage array and used to modulate the pixel elements in the time domain. Such systems are often called pulse-width-modulation (PWM) systems. For example, a 50%

brightness value stored in a storage array may entail turning the pixel cell on for half of a frame time and then off for the second half of the frame time.

In other cases, a digital to analog converter may convert data from the memory to an analog gray scale format for use by a pixel array. For example, an entire column or more of pixel values may be read from the storage array into an on-chip register. These values may be converted to analog values in parallel and driven into the pixel array.

One electro-optical device 10 which may not need a periodic display refresh in some embodiments, is illustrated in Fig. 5. If the periodic display refresh is eliminated, this may also increase the available system wide bandwidth. The illustrated embodiment uses integrated memory 60 for each pixel cell 12. In some embodiments, pixel information may be passed through a digital to analog converter (DAC) 62 to produce gray scale information. The particular manner in which pixels are arranged in the storage array and converted to analog signals may vary by implementation.

Each pixel metal electrode or top metal 12 may be coupled to a separate DAC 62. In one embodiment of the present invention, the DAC may be an eight bit DAC coupled to eight one bit storage elements 60. Each storage element 60 may, for example, be a static random access memory (SRAM) cell. Each one bit storage element 60 may be

coupled by a transfer transistor 58 to a different row 56 and a column 54. Thus, the information which is used to refresh the metal mirror 12 may be stored in the memory 60. When it is desired to change the pixel information to change the displayed image, then the information in the memory 60 is refreshed.

Since the display refresh controller only needs to refresh new information to the display, the overall drain on the computer system including the buses and memory may be reduced, potentially yielding better performance out of the other components in the computer system which rely on these limited resources. In addition, the amount of redundant information flowing to the display may be reduced, allowing more new information to be sent to the display. This potentially enables the display of higher resolution or higher rate images.

In one embodiment of the present invention, a projection display 64 includes the spatial light modulators 66, 74 and 76, using liquid crystal over silicon technology with integrated memory. The reflective liquid crystal display projection system 64 typically includes a modulator or display panel (LCD display panels 74, 66 and 76) for each primary color that is projected onto a screen 92. In this manner, for a red-green-blue (RGB) color space, the projection system 64 may include an LCD display panel 74 that is associated with a red color band, an LCD display

panel 66 that is associated with the green color band and LCD display panel 76 that is associated with the blue color band. Each of the LCD display panels 66, 74 and 76 modulates light from the light source 94 and the optics 96 that form red, green and blue images, respectively, and add together to form a composite color image on the screen 92. To accomplish this, each LCD display panel receives electrical signals indicating the corresponding modulated beam image to be formed.

More particularly, the projection display 64 may include a beam splitter 86 that directs a substantially collimated white beam 98 of light, provided by the light source 94, to optics that separate the white beam 98 into red 82, blue 78 and green 102 beams. In this manner, the white light beam 98 may be directed to a red dichroic mirror 72 that reflects the red beam towards the LCD display panel 74 that, in turn, modulates the red beam 82. The blue beam passes through the red dichroic mirror to a blue dichroic mirror 70 that reflects the blue beam towards the LCD panel 76 for modulation. The green beam 102 passes through the red and blue dichroic mirrors for modulation by the LCD display panel 66.

For reflective LCD display panels, each LCD display panel 66, 74 and 76 modulates the incident beam and reflects the modulated beams 90, 100 and 68 respectively, so that the modulated beams return on the paths described

above to the beam splitter 86. The beam splitter 86, in turn, directs the modulated beams through projection optics such as a lens 88, to form modulated beam images that ideally overlap and combine to form the composite image on the screen 92. Each of the panels 66, 74, and 76 may be implemented using liquid crystal over semiconductor technology as illustrated for example in Fig. 2.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. For example, while a projection display is described, the present invention may be used in direct view displays as well. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A display comprising:

a semiconductor substrate;

a liquid crystal over semiconductor pixel array formed in said substrate; and

a memory coupled to said array, said memory also formed in said substrate.

2. The display of claim 1 wherein said pixel array includes a plurality of pixels each including a memory cell.

3. The display of claim 2 wherein said memory cells are static random access memory cells.

4. The display of claim 1 wherein said pixel array is coupled to said memory by a digital to analog converter.

5. The display of claim 1 wherein said memory includes a cell associated with each of a plurality of pixels of the pixel array.

6. The display of claim 1 wherein said pixel array forms a reflective liquid crystal spatial light modulator.

7. The display of claim 1 wherein said memory a dynamic random access memory, and said display includes a

refresh circuit, said refresh circuit adapted to refresh both said dynamic random access memory and said pixel array.

8. The display of claim 1 wherein said pixel array is adapted to eliminate the need for a periodic pixel refresh cycle.

9. A method for displaying information comprising:

forming a pixel array in a liquid crystal over semiconductor substrate; and

forming a memory in said liquid crystal over semiconductor substrate, with said memory coupled to said pixel array.

10. The method of claim 9 wherein forming a memory includes forming a memory associated with each pixel of said pixel array.

11. The method of claim 9 wherein forming a memory includes forming a volatile memory and refreshing said volatile memory and said pixel array in the same refresh cycle.

12. The method of claim 9 including displaying information without using a periodic refresh cycle.

13. A display comprising:

a memory array;

a pixel array; and

a refresh circuit coupled to said memory array and said pixel array, said refresh circuit adapted to refresh said memory array and said pixel array.

14. The display of claim 13 wherein said memory array and said pixel array are formed in the same semiconductor substrate with said refresh circuit.

15. The display of claim 14 wherein said substrate is a liquid crystal over semiconductor substrate, said pixel array including a plurality of electrodes adapted to interact with a liquid crystal material over said pixel array.

16. The display of claim 13 wherein said memory array is formed of dynamic random access memory.

17. A method for displaying information comprising:

providing a pixel array in a semiconductor substrate;

providing a memory array in said substrate; and

refreshing said memory array and said pixel array in the same refresh cycle.

18. The method of claim 17 including forming said memory and pixel arrays in a liquid crystal over semiconductor substrate.

19. The method of claim 17 including storing pixel data in said memory array.

20. The method of claim 17 including providing a liquid crystal material over said pixel array.

21. A processor-based system comprising:

a processor;

an interface bus coupled to said processor; and

a display coupled to said processor, said display including a liquid crystal over semiconductor substrate, said substrate including a memory array and a pixel array coupled to said memory array.

22. The system of claim 21 wherein said memory array includes a plurality of cells, each cell coupled to a pixel of said pixel array.

23. The system of claim 22 wherein said memory cells are static random access memory cells.

24. The system of claim 23 wherein said pixel array is a reflective liquid crystal array.

25. The system of claim 24, said memory including a plurality of storage locations at each pixel and a digital to analog converter coupling each of said storage locations to a different pixel cell.

LIQUID CRYSTAL OVER SEMICONDUCTOR
DISPLAY WITH ON-CHIP STORAGE

Abstract of the Disclosure

A display device, such as a projector system, may include a plurality of display panels formed from liquid crystal over semiconductor substrates which incorporate not only the pixel elements but memory as well. The presence of memory in the display allows a host system, such as a computer, to send only new picture information to the display and avoid the transmission of information that does not change. Thus, the display update bandwidth required of the host system may be reduced, allowing the host system to use resources typically required by the display update process for improved performance of other operations. In addition, the elimination of redundant information being transmitted to the display may allow more new information to be transmitted, enabling, for example, a higher resolution display.

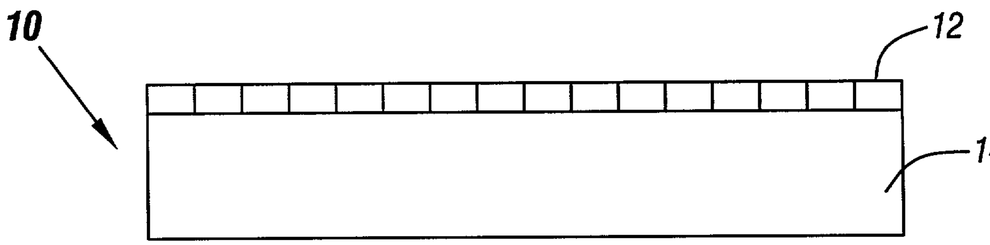


FIG. 1

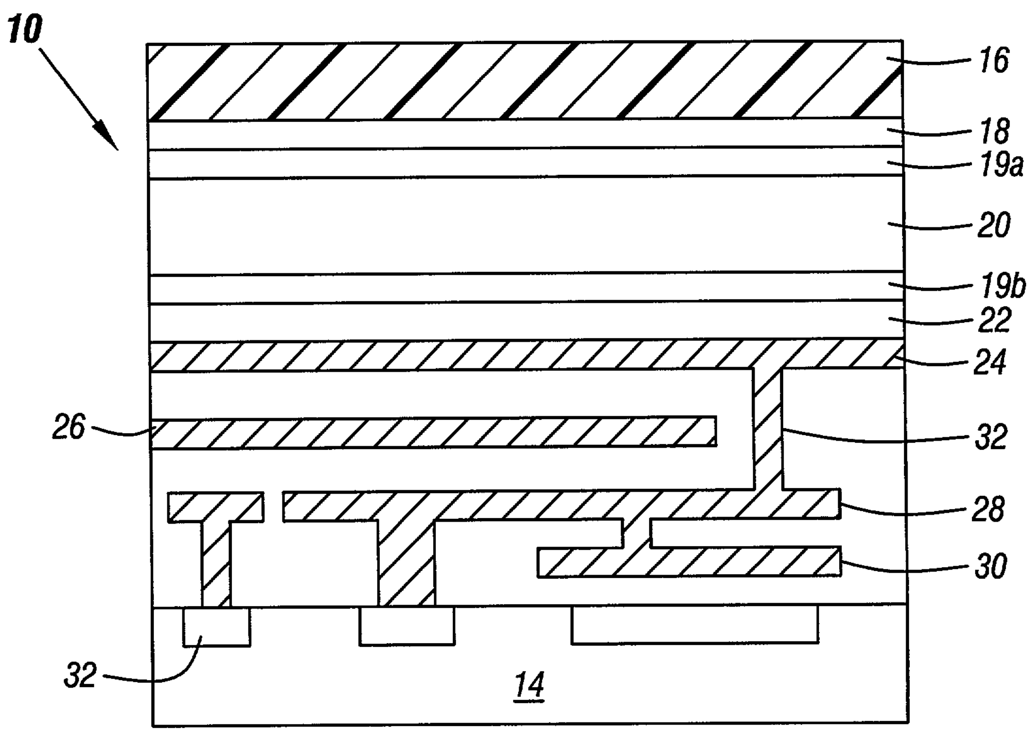


FIG. 2

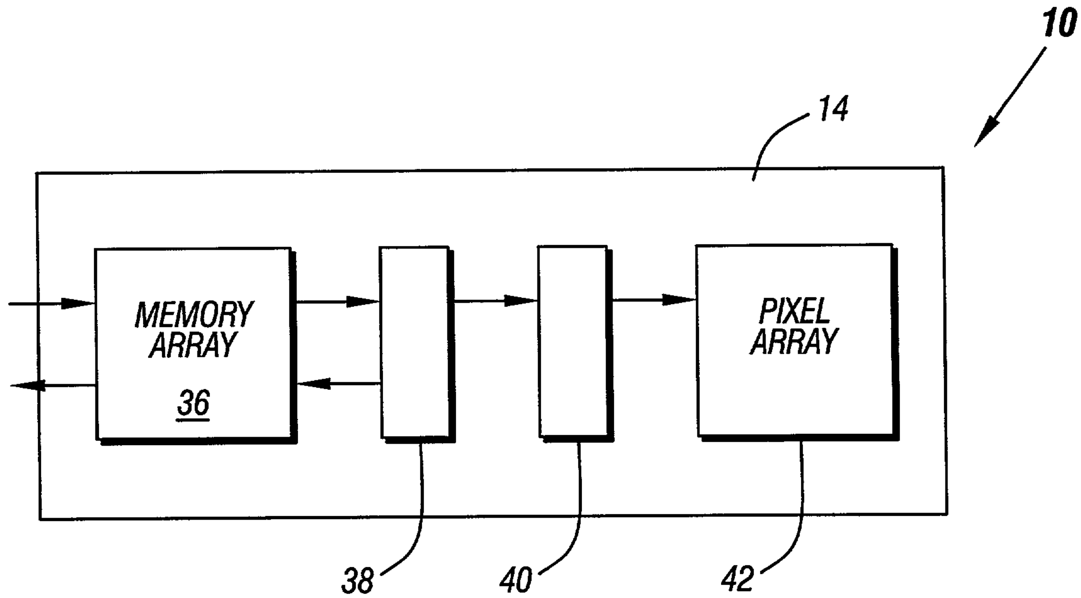

10
14
MEMORY ARRAY
36
PIXEL ARRAY
38
40
42

FIG. 3

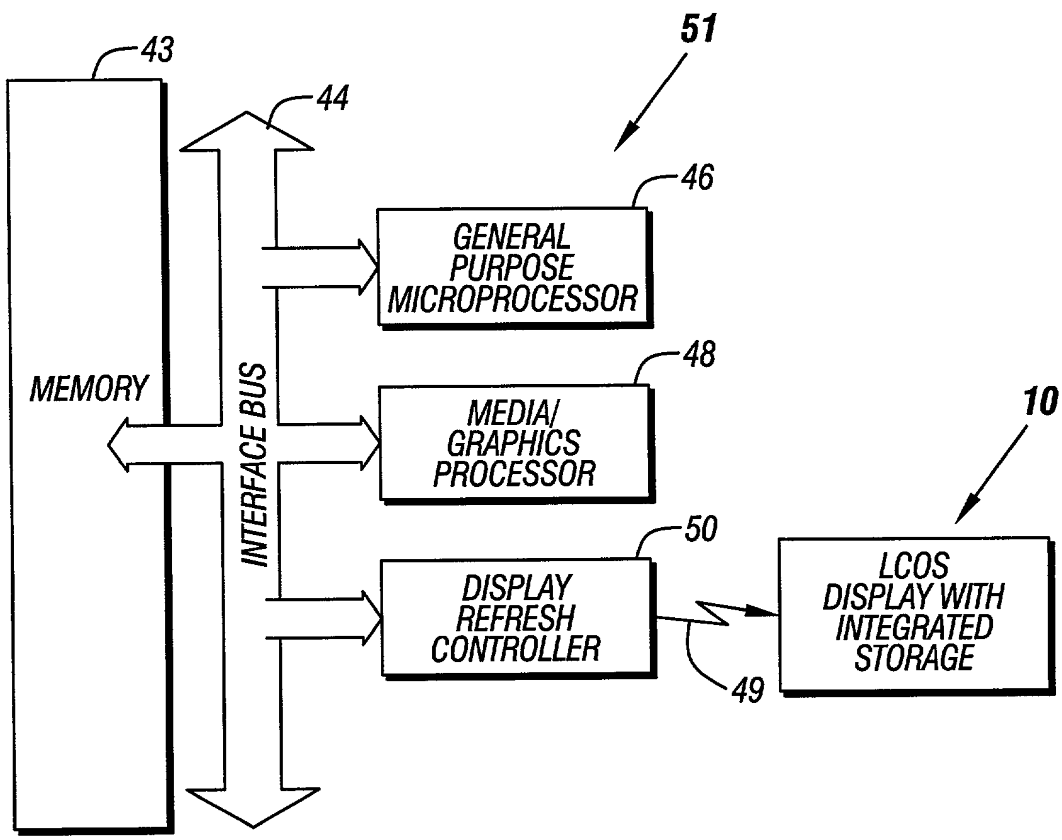
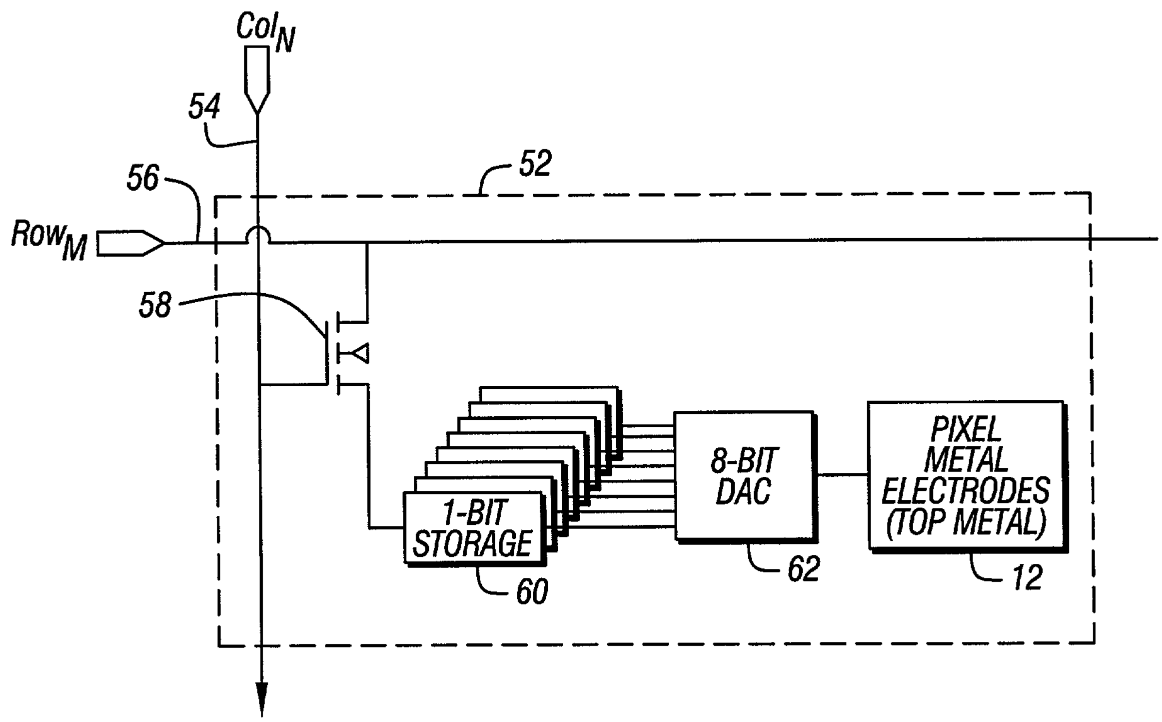
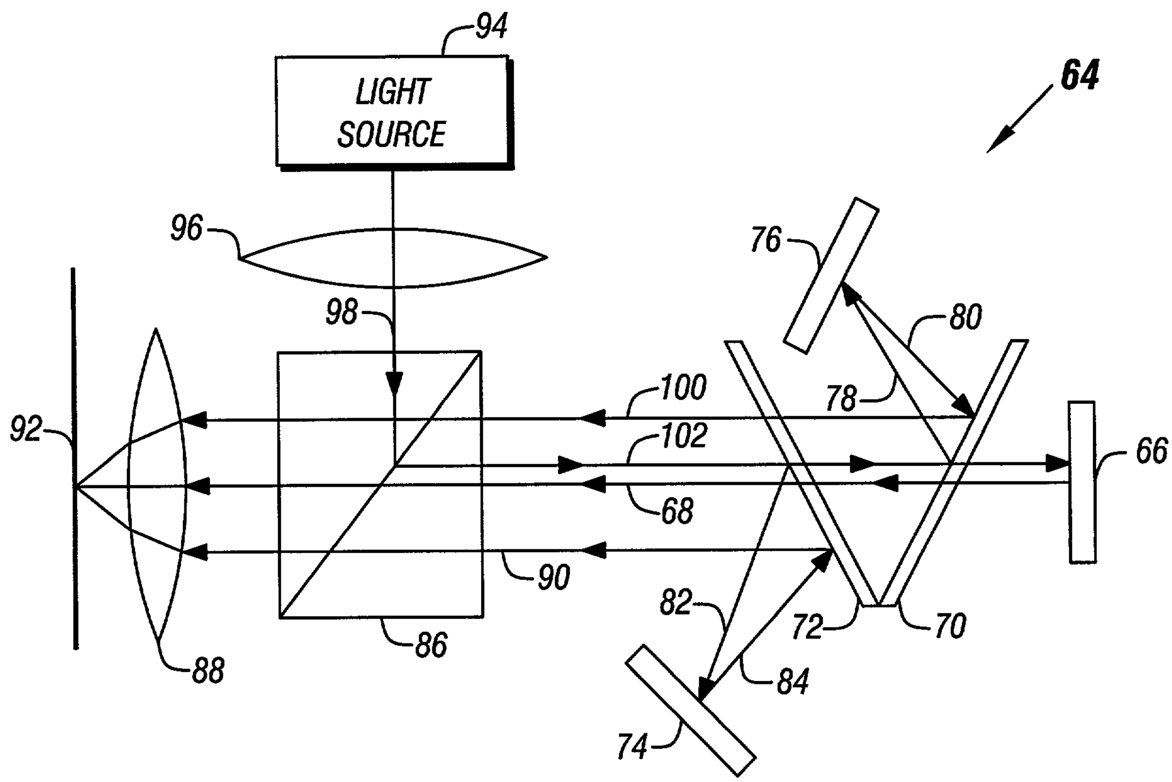

43
44
51
46
GENERAL PURPOSE MICROPROCESSOR
MEMORY
INTERFACE BUS
48
MEDIA/ GRAPHICS PROCESSOR
10
50
DISPLAY REFRESH CONTROLLER
LCOS DISPLAY WITH INTEGRATED STORAGE
49

FIG. 4



Col$_N$
54
56
52
Row$_M$
58
1-BIT
STORAGE
60
8-BIT
DAC
62
PIXEL
METAL
ELECTRODES
(TOP METAL)
12

FIG. 5



94
LIGHT
SOURCE
64
96
76
98
80
100
78
92
102
66
68
90
82
72
70
86
88
84
74

FIG. 6

Attorney's Docket No.: INTL-0219 -US (P7127) PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

LIQUID CRYSTAL OVER SEMICONDUCTOR DISPLAY WITH ON-CHIP STORAGE

the specification of which

X	is attached hereto.
	was filed on ____________ as
	United States Application Number ____________
	or PCT International Application Number ____________
	and was amended on ____________
	(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate Issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			Priority Claimed	
Number	(Country)	(Day/Month/Year Filed)	Yes	No
Number	(Country)	(Day/Month/Year Filed)	Yes	No
Number	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of the United States provisional application(s) listed below:

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Number)	Filing Date	(Status-patented, pending, abandoned)
(Application Number)	Filing Date	(Status-patented, pending, abandoned)

I hereby appoint Timothy N. Trop, Reg. No. 28,994; Fred G. Pruner, Jr., Reg. No. 40,779, Dan C. Hu, Reg. No. 40,025; Coe F. Miles, Reg. No. 38,559, and John R. Merkling, Reg. No. 31,716 my patent attorneys, of TROP, PRUNER, HU & MILES, P.C., with offices located at 8554 Katy Freeway, Ste. 100, Houston, TX 77024, telephone (713) 468-8880, and Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Sean Fitzgerald, Reg. No. 32,027; David J. Kaplan, Reg. No. 41,105; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; and Charles K. Young, Reg. No. 39,425; my patent attorneys, of INTEL CORPORATION; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Timothy N. Trop, TROP, PRUNER, HU & MILES, P.C., 8554 Katy Freeway, Ste. 100, Houston, TX 77024 and direct telephone calls to Timothy N. Trop , (713) 468-8880.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: **SCOTT A. ROSENBERG**	
Inventor's Signature: Scott A Rosenberg	Date: 6/28/99
Residence: **PALO ALTO, CALIFORNIA**	Citizenship: **U.S.A.**
Post Office Address: **875 UNIVERSITY AVENUE, APARTMENT 9, PALO ALTO, CALIFORNIA 94301**	
Full Name of Second/Joint Inventor: **ANTHONY C. MILLER**	
Inventor's Signature: Anthony C. Miller	Date: 7/1/99
Residence: **GILBERT, ARIZONA**	Citizenship: **U.S.A.**
Post Office Address: **1811 E. LEXINGTON AVENUE, GILBERT, ARIZONA 85234**	

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